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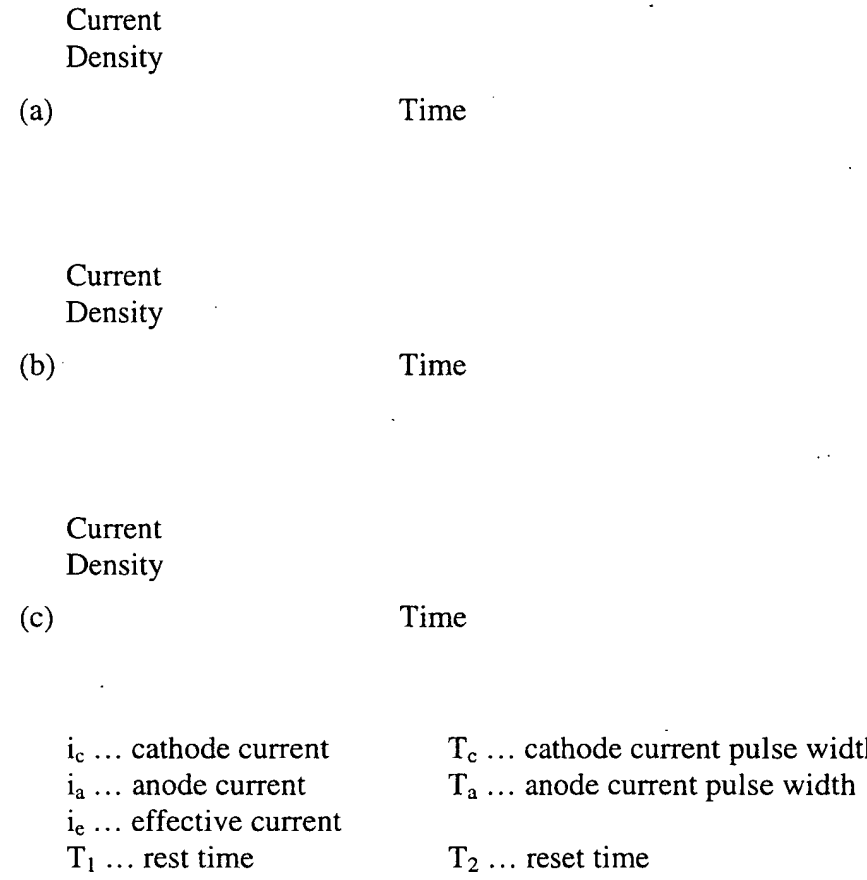
(57) [Abstract]

[Purpose] To ultimately pack a metallic conductor in only the holes and channels without gaps and at a higher density than in prior art when applying metallization to a dielectric surface having holes and channels formed in a pattern in the production process of a high-density, thin-film, multilayer circuit board, and to make this conductive surface uniform and coplanar with the surface containing the above-mentioned dielectric surface. In addition, to facilitate multilayering a thin-film circuit by forming a vertical layout by the resulting flattened via, and to greatly improve mounting density while maintaining high yield.

[Constitution] In a thin-film circuit production method having an electrolysis system for working a thin-film circuit by electrolysis using the thin-film circuit board as one of the electrodes, the dielectric

surface of the above-mentioned thin-film circuit is subjected to electroplating by current reversal electrolysis alternating cathode electrodeposition and anode dissolution, and unnecessary metal is removed by electroetching or electropolishing.

Figure 2



i_c ... cathode current
i_a ... anode current
i_e ... effective current
T_1 ... rest time
T_c ... cathode current pulse width,
T_a ... anode current pulse width
T_2 ... reset time

[Claims]

[Claim 1] Thin-film circuit production method, comprising a thin-film circuit production method having an electrolysis system for working a thin-film circuit by electrolysis using the thin-film circuit board as one of the electrodes,

and characterized by subjecting the dielectric surface of the above-mentioned thin-film circuit to electroplating by current reversal electrolysis alternating cathode electrodeposition and anode dissolution.

[Claim 2] Thin-film circuit production method, comprising a thin-film circuit production method having an electrolysis system

for working a thin-film circuit by electrolysis using the thin-film circuit board as one of the electrodes,

and characterized by subjecting a metallic film on the dielectric surface of the above-mentioned thin-film circuit to electroetching or electropolishing by current reversal electrolysis alternating cathode electrodeposition and anode dissolution.

[Claim 3] Thin-film circuit production method described in either Claim 1 or Claim 2, characterized by the current used in the above-mentioned current reversal electrolysis having a pulse waveform.

[Claim 4] Thin-film circuit production method described in Claim 3, characterized by inserting a rest time in which no current flows in the above-mentioned electrolysis system between the time of the above-mentioned cathode electrodeposition and the time of the above-mentioned anode dissolution.

[Claim 5] Thin-film circuit production method described in either Claim 1 or Claim 2, characterized by the current used in the above-mentioned current reversal electrolysis having an asymmetrical sine waveform.

[Claim 6] Thin-film circuit production method described in any of Claims 1 through 5, characterized by the current used in the above-mentioned current reversal electrolysis having a frequency of 1 Hz to 1 MHz and an effective current of $\forall$ 0.1 A/dm^2 to $\forall$ 10 A/dm^2 (both signs either positive or negative).

[Claim 7] Thin-film circuit production method, characterized by packing a metal by electroplating by the thin-film circuit production method described in Claim 1 in the holes or channels of a thin-film circuit board containing a dielectric having holes or channels formed in a pattern, and forming the above-mentioned dielectric surface flat and coplanar with the surface of the above-mentioned packed metal by removing unnecessary metal by electroetching by the thin-film circuit production method described in Claim 2.

[Claim 8] Thin-film circuit board, characterized by packing a metal by electroplating by the thin-film circuit production method described in Claim 1 in the holes or channels of a thin-film circuit board containing a dielectric having holes or channels formed in a pattern, and forming the above-mentioned dielectric surface flat and coplanar with the surface of the above-mentioned packed metal by removing unnecessary metal by electroetching by the thin-film circuit production method described in Claim 2.

[Claim 9] Thin-film multilayer circuit board, comprising a thin-film multilayer circuit board formed by repeating a step for forming a dielectric film, a step for finely working said dielectric film, and the thin-

film circuit production method described in Claim 7, and characterized by the above-mentioned packed metal forming a via and this via comprising a layout connected vertically across many layers.
[Claim 10] Electronic circuit device, formed by connecting an integrated circuit to the thin-film multilayer circuit described in Claim 9 by way of a minute solder ball.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Application]

This invention pertains to a thin-film circuit production method by current reversal electrolysis and a thin-film circuit board, thin-film multilayer circuit board, and electronic circuit device using this. In particular, as an ideal thin-film circuit production method for flattening elements such as via and channels, this invention pertains to production processes using multilayer circuit boards for mounting LSI and LSI electronic circuit devices, which are steadily becoming higher density and higher speed year by year.

[0002]

[Prior Art]

With the ever greater processing capacity of LSI devices, LSI by prior art have become multi-pin, and as signal startup speed becomes ever faster, high-speed performance is demanded of signal transmission circuits. In response to these demands, multi-chip mountings that overcome the mode of mounting a single chip package on a printed substrate and use a simultaneously sintered multilayer substrate comprised of a ceramic-metal conductor for the mounting substrate have become the mainstream, especially in super high-speed systems typified by large computers and supercomputers (for example, *Nikkei Microdevices*, November 1990 issue, p. 145).

[0003]

Methods that have been studied as a means for further increasing the performance of mounting circuit boards in the future include using an organic resin having a low dielectric constant as an interlayer insulating material, using copper having high conductivity as the layout conductor, and increasing layout density by using high-precision photolithography for layout pattern formation. Furthermore, multilayering of circuits is essential for achieving a high-density layout, and increasing the sectional aspect ratio of the layout is necessary if increased layout density and reduced layout resistance are to be achieved.

[0004]

Many methods have been offered already for forming a thin-film multilayer circuit board comprised of copper and an organic resin in this way.

[0005]

One important element cited as characterizing the mode of thin-film multilayer circuits is the shape and formation method of the via charged with connecting between upper and lower layers. That is, it is no exaggeration to say that the shape and formation method of via have the greatest effect on interlayer connection reliability and mounting density.

[0006]

This via shape will be explained below using Figure 8. Figure 8 is a diagram showing contrasting sections of thin-film multilayer circuits having via.

[0007]

As shown in Figure 8, via are broadly divided into two shapes. In the first, shown in Figure 8(a), the via shape is not flat on top.

[0008]

Hereafter, this is called an "unflattened via." Because the center of the via hole is not completely packed with a conductor in this case, a resulting depression is left immediately after forming the via. This depression is more or less flattened by packing to some extent with an organic resin when the layer above this is formed, but this flattening is generally not complete. This lack of flatness has a number of effects on the series of thin-film steps, and restricts circuit board design.

[0009]

For example, this depression makes it impossible to form via in the same location vertically. Therefore, when using unflattened via, via must be formed by offsetting the formation position in each layer by at least the diameter of the via. As a result, the effective area of the whole substrate occupied by via is increased, and becomes a bottleneck to improving mounting density. In addition, the above-mentioned depression causes problems such as leaving photoresist developing residue in the step for laminating an upper thin-film layer above this or etching residue during layout working, and becomes a factor reducing yield.

[0010]

An example of this unflattened via is given in *IEEE International Electronic Manufacturing Technology Symposium*, pp. 177-183 (1987) [Example 1]. In this example, a photosensitive polyimide is used as an interlayer insulating film, a copper electroplating film is used as the layout conductor, and a thin-film multilayer substrate is formed by a sequential lamination process. Because the shape of the via

connecting between layers in this method is as shown in Figure 8(a), this makes it difficult to greatly improve mounting density as demanded in the future.

[0011]

In the second via shape, shown in Figure 8(b), the via hole is completely packed with the layout conductor up to the same plane as the surface of the insulating layer. This is called a "flattened via." In this case, via in the same vertical location can be connected, making this an ideal configuration for improving mounting density. This also has the advantages that there is no effect on thin-film steps due to surface irregularities, and reduced yield is not a problem. Therefore, this flattened via is preferred over the above-mentioned unflattened via from the standpoint of improved mounting density and improved yield.

[0012]

Examples of this flattened via include *Proceedings of 1989 International Electronic Packaging Symposium*, pp. 248-270 [Example 2], *Proceedings of 41st Electronic Components & Technology Conference*, pp. 689-692 [Example 3], and the technique described in Japan Unexamined Patent No. 5-218645 [Example 4].

[0013]

[Problems that the Invention is to Solve]

As described above, using flattened via on a thin-film multilayer circuit board is preferred from the standpoint of improved mounting density and improved yield. Examples 2 to 4 of prior art cited above describe this flattened via. However, these prior art examples have the following problems:

[0014]

In Example 2, a via is worked by dry etching by oxygen plasma using a photosensitive polyimide as an interlayer insulating film. Next, a via conductor is grown from the surface of the lower-layer layout appearing on the via floor by electroless nickel plating, plating is stopped when it becomes coplanar with the surface of polyimide, and the shape shown in Figure 8(b) is obtained. The most important requirement in this case is that the entire surface of via nickel can be ultimately formed at a uniform height and without defects. However, electroless plating is affected by the electric potential of the plating growth surface. As a result, plating deposition speed often differs due to a different electrical environment in the layout beneath the via floor (for example, whether this is electrically independent or electrically connected), and it becomes an extremely difficult problem to pack a conductor without defects in all of the innumerable fine via present within a plane.

[0015]

In Example 3, a via is worked by ablation by an excimer laser, still using polyimide as an

interlayer insulating film. Next, the conductor material copper is deposited on the entire substrate surface and completely packs the via. During this, the same thickness of copper adheres on top of the polyimide film around the via. Because this copper on top of polyimide is unnecessary, it is completely removed by chemical mechanical polishing (CMP), and polishing is stopped at the point when it reaches the polyimide surface. As a result, the shape shown in Figure 8(b) is obtained. This process has the advantage that the shape shown in Figure 8(b) can be formed securely, but has the drawback that the chemical mechanical polishing step is expensive. In addition, as the number of thin-film circuit layers is increased, substrate warping reaches a level that cannot be ignored. This leads to the problem that parts such as the polishing plate of the polishing apparatus cannot track this substrate warpage, leaving parts with residual copper on top of polyimide within the plane and causing a risk of layout shorting.

[0016]

When forming a thin-film multilayer circuit board comprised of organic resin and layout copper in Example 4, first, a Cr/Cu laminated film (meaning that the underlayer is comprised of the two layers of Cr and Cu; likewise below) is sputtered and grown as an electroplating underlayer on the entire thin-film surface after via working, the via is packed by subjecting the entire surface to copper electroplating, and the surface is flattened. Next, this copper electroplating film is subjected to wet etching and excess copper is removed, leaving only the layout thickness. However, because it does not achieve complete flattening of the depression in the via, but leaves a layout step part, this method has the problem that it risks causing restrictions in terms of forming vertically connected via and the number of layers that can be multilayered.

[0017]

Therefore, to realize the high-density thin-film circuit boards of the future, it would be desirable to establish a fine thin-film circuit formation process that can form flattened via by a low-cost, secure method and can facilitate multilayering.

[0018]

This invention was developed to solve the problems in prior art described above. Its purpose is to offer a method that ultimately packs a metallic conductor in only the holes and channels without gaps and at a higher density than in prior art when applying metallization to an entire dielectric surface having holes and channels formed in a pattern in the production process of a high-density, thin-film, multilayer circuit board, and makes this conductive surface uniform and coplanar with the surface containing the above-mentioned dielectric surface. An additional purpose is to achieve a completely flat

surface in each layer comprising a thin-film multilayer circuit, facilitate multilayering a thin-film circuit, and greatly improve mounting density while maintaining high yield.

[0019]

[Means of Solving the Problems]

The first constitution of a thin-film circuit production method with which this invention is concerned for achieving the purposes given above comprises a thin-film circuit production method having an electrolysis system for working a thin-film circuit by electrolysis using the thin-film circuit board as one of the electrodes, and is characterized by subjecting the dielectric surface of the above-mentioned thin-film circuit to electroplating by current reversal electrolysis alternating cathode electrodeposition and anode dissolution.

[0020]

The second constitution of a thin-film circuit production method with which this invention is concerned for achieving the purposes given above comprises a thin-film circuit production method having an electrolysis system for working a thin-film circuit by electrolysis using the thin-film circuit board as one of the electrodes, and is characterized by subjecting a metallic film on the dielectric surface of the above-mentioned thin-film circuit to electroetching or electropolishing by current reversal electrolysis alternating cathode electrodeposition and anode dissolution.

[0021]

More particularly, the first and second constitutions of thin-film circuit production methods described above are characterized by the current used in the above-mentioned current reversal electrolysis having a pulse waveform.

[0022]

Still more particularly, the current reversal electrolysis method using a pulse waveform current described above is characterized by inserting a rest time in which no current flows in the above-mentioned electrolysis system between the time of the above-mentioned cathode electrodeposition and the time of the above-mentioned anode dissolution.

[0023]

Separately and more particularly, the first and second constitutions of thin-film circuit production methods described above are characterized by the current used in the above-mentioned current reversal electrolysis having an asymmetrical sine waveform.

[0024]

In terms of current conditions, this method may be characterized by the current used in the

above-mentioned current reversal electrolysis having a frequency of 1 Hz to 1 MHz and an effective current of $\forall$ 0.1 A/dm^2 to $\forall$ 10 A/dm^2 (both signs either positive or negative).

[0025]

Expressed more concretely, the method is characterized by packing a metal by electroplating by a thin-film circuit production method having the first constitution described above in the holes or channels of a thin-film circuit board containing a dielectric having holes or channels formed in a pattern, and forming the above-mentioned dielectric surface flat and coplanar with the surface of the above-mentioned packed metal by removing unnecessary metal by electroetching by a thin-film circuit production method having the second constitution described above.

[0026]

The constitution of a thin-film circuit board with which this invention is concerned is characterized by packing a metal by electroplating by a thin-film circuit production method having the first constitution described above in the holes or channels of a thin-film circuit board containing a dielectric having holes or channels formed in a pattern, and forming the above-mentioned dielectric surface flat and coplanar with the surface of the above-mentioned packed metal by removing unnecessary metal by electroetching by a thin-film circuit production method having the second constitution described above.

[0027]

The constitution of a thin-film circuit board with which this invention is concerned comprises a thin-film multilayer circuit board formed by repeating a step for forming a dielectric film, a step for finely working said dielectric film, and the thin-film circuit production method described above for working metal in holes or channels of a dielectric, and is characterized by the above-mentioned packed metal forming a via and this via comprising a layout connected vertically across many layers.

[0028]

Finally, an electronic circuit device with which this invention is concerned is formed by connecting an integrated circuit to the thin-film multilayer circuit described above by way of a minute solder ball.

[0029]

[Operation]

By using current reversal electrolysis alternating cathode electrodeposition and anode dissolution when working a substrate surface having a fine hole or channel pattern by electrolysis, the diffusion layer on the substrate surface used as the electrode in the first-stage electroplating process becomes thinner than by direct-current electrolysis. As a result, the plating film layer adhering to the substrate

surface during cathode electrodeposition can be formed flat and uniform compared to direct-current electrolysis regardless of irregularities on the substrate surface. Dissolving metal preferentially from the metal projection adhering to the substrate surface during anode dissolution increases plating film uniformity even more. Inserting a rest time in which no current flows between cathode electrodeposition and anode dissolution has the effect of increasing plating film uniformity of this diffusion layer even more.

[0030]

Electroetching by current reversal electrolysis as a second stage has the effect of removing unnecessary metal from the dielectric surface and making metal deposited in holes or channels flat and coplanar with the dielectric surface.

[0031]

Repeating a first-stage electroplating step and a second-stage electroetching step has the effect of making the plating film layer more precisely uniform.

[0032]

Furthermore, when via surface uniformity is improved by applying this method to flattened via, a configuration vertically overlapping flattened via when formed on a thin-film multilayer circuit board can be produced with greater reliability, producing an effect improving mounting density.

[0033]

[Working Examples]

Working examples pertaining to this invention are explained below using Figures 1 through 7.

[Configuration of Electrolysis System for Reducing This Invention to Practice]

First, the configuration of an electrolysis system for reducing this invention to practice will be explained using Figure 1. Figure 1 is a schematic figure showing the configuration of an electrolysis system for implementing the electrolysis with which this invention is concerned.

[0034]

The configuration of this electrolysis system is comprised of control personal computer 511, desired signal waveform generator 512, constant-current constant-voltage pulse source 513, and electrolytic bath 514. In addition, electrolytic bath 514 is filled with electrolyte solution 515, and contains substrate holder and substrate 516 opposite counter-electrode 517.

[0035]

Constant-current constant-voltage pulse source 513 applies a voltage to the opposing electrodes in electrolytic bath 514. Applying a voltage precipitates metal in electrolyte solution 515 onto substrate holder and substrate 516 and plates its surface, or dissolves metal into electrolyte solution 515 and

etches its surface, depending on whether this surface is a negative electrode or a positive electrode.

[0036]

Desired signal waveform generator 512 generates the desired current waveform, and inputs the current waveform generated to constant-current constant-voltage pulse source 513.

[0037]

Control personal computer 511 is inputted parameters for determining the waveform by the read program, and as a result, generates the desired current waveform by driving desired signal waveform generator 512.

[0038]

[Current Reversal Electrolysis]

Next, the current reversal electrolysis with which this invention is concerned will be explained using Figures 2 through 4. Figure 2 is a graph showing the correlation between current density and time in current reversal electrolysis with which this invention is concerned. Figure 3 is a schematic diagram contrasting an electrolytic bath with its metal concentration. Figure 4 is a diagram contrasting how the surface on a substrate varies when plated by direct current or a pulse current.

[0039]

This current reversal electrolysis is a technique that forms an electroplating underlayer on the surface of a substrate having a pattern of fine holes or channels. First, a uniform and flat plated film is formed on the entire surface by electrolyzing by a waveform causing mainly cathode electrodeposition. After this, a conductor metal is embedded flat in only the fine holes or channels by etching the plating film uniformly over the entire surface by electrolyzing by a waveform causing mainly anode dissolution.

[0040]

This is explained in detail below: Typical reversal pulse waveforms are shown in Figures 2(a) to (c). Needless to say, waveforms other than these can be used, and these waveforms (a) to (c) can also be combined as appropriate and used.

[0041]

First, the correlation of the current used in electrolysis with cathode electrodeposition and anode dissolution will be explained. In Figure 2, current i_c on the negative side is the cathode current. When this current is flowing, the phenomenon of cathode electrodeposition (plating film deposition) occurs on substrate holder and substrate 516.

[0042]

Current i_a on the positive side is an anode current, which causes the phenomenon of anode dissolution (plating film dissolution) on substrate holder and substrate 516. That is, in the current

reversal electrolysis with which this invention is concerned, deposition of plating film on the substrate surface proceeds during T_c (cathode current pulse width) when the cathode current is flowing, and dissolution of plating film on the substrate surface proceeds during T_a (anode current pulse width) when the anode current is flowing.

[0043]

In Figure 2(a), plating film deposition and plating film dissolution occur alternately by the cathode current and anode current described above flowing in alternate pulses. In addition, the waveform of Figure 2(b) has set rest times (times of zero current) T_1 and T_2 inserted after the cathode current pulse and the anode current pulse in the reversal pulse waveform of Figure 2(a).

[0044]

Rest times are introduced to promote phenomena such as crystallization of deposited metal, recovery of diffusion layer concentration, and absorption/desorption equilibrium of additives in the plating solution, and affects plating film quality.

[0045]

Furthermore, Figure 2(c) is an asymmetrical sine wave (a wave superimposing alternating current and direct current). The fact that the first and last transition peaks of the current are gentle means that effects such as occur during the pulse waveforms of Figures 2(a) and (b) described above appearing in the cathode electrodeposition process and anode dissolution process described above produce different properties in the plating film.

[0046]

Next, phenomena occurring during electroplating using these current waveforms as the first stage will be explained in detail using Figures 3 and 4 in addition to Figure 2.

[0047]

All of the waveforms in Figures 2(a), 2(b), and 2(c) produce repetition of electrodeposition and dissolution on the micro level, but the effective current [$i_e = (i_c T_c - i_a T_a) / (T_c + T_a)$] becomes negative; that is, the sign of the cathode current. This results in an increase in current contributing to plating film deposition, with the end result that the overall response is deposition of plating film. However, the actual phenomena occurring at the electrode surface differ greatly from direct-current plating by prior art.

[0048]

To show this, first, the concepts "plating solution bulk" and "diffusion layer" will be explained. The concentration of metallic ions in plating solution is not uniform at all locations. In particular, locations near the solid surface contacting the plating solution are affected by factors such as the polarity and wettability of this solid surface, and the concentration of components in the plating solution differs

between the part affected by this (called "plating solution bulk") and locations far from the solid surface.

[0049]

In particular, during the electrodeposition process, metallic ions in the electrolyte solution contacting the surface where electrodeposition occurs (the deposited surface) are constantly taken up by the deposited surface. As a result, the concentration of metallic ions in the solution near the deposited surface becomes rather lower than the concentration of metallic ions in the plating solution bulk. This region of low metallic ion concentration is called a "diffusion layer."

[0050]

Figure 3(a) schematically shows an electrolytic bath during plating by electrolysis, and Figure 3(b) shows the correlation between metallic ion concentration and the distance from the electrode being plated.

[0051]

During electrolysis by a pulse current such as that in Figure 2(a), metal is deposited and the electrode surface is plated only in the short time of time T_c when cathode current pulse i_c is flowing. That is, during this time T_c, only metallic ions drawn from the solution to the deposited surface by an electric field and arriving at the deposited surface receive electrons and are precipitated.

[0052]

As this progresses, the concentration of metallic ions in the plating solution on the deposited surface drops, producing the diffusion layer described above. However, this diffusion layer is thinner using a pulse current compared to electrodeposition by a constant current constantly supplying electrons to the electrode.

[0053]

Furthermore, when pulse rest times are inserted as in Figure 2(b), metallic ions are not drawn to the electrode during these rest times. As a result, the metallic ion concentration of the diffusion layer recovers due to random thermal diffusion motion of these metallic ions. This type of phenomenon of the metallic ion concentration of the diffusion layer recovering also results in making the diffusion layer thinner.

[0054]

The substrate surface has minute irregularities such as shown in Figure 4. When a substrate surface having irregularities is electrolyzed and plated by a direct current, metallic ions are diffused and supplied to depressions more slowly than to projections, as shown in Figure 4(a). Therefore, the diffusion layer in depressions is thinner than the diffusion layer on projections. As a result, the plating film tends to be thinner in depressions than on projections, leading to non-uniform thickness. When

electrolyzed and plated by a pulse current as shown in Figures 2(a) and (b), the thickness of the diffusion layer is thin and more or less uniform regardless of location, as shown in Figure 4(b). Consequently, plating film thickness is also uniform.

[0055]

As explained above, metal is deposited only during time T_c when cathode current i_c in Figures 2(a) to (c) is flowing.

[0056]

During the following time T_a when anode current i_a is flowing, metal already deposited is dissolved and the diffusion layer concentration recovers. Projecting parts of the plating film surface dissolve preferentially during this due to the concentrated electric field. As a result, the plating film surface is smoothed. Therefore, by plating using the current reversal electrolysis shown in Figure 2, a plating film of uniform thickness can be formed over the entire surface, especially on a dielectric surface having depressions such as holes or channels, and by completely filling these depressions, a flat metallic reverse surface can ultimately be obtained over the entire surface.

[0057]

Except for small differences in experimental conditions, the behavior described above is the same using any of the current waveforms in Figure 2. Therefore, all of these waveforms can obtain the same effects.

[0058]

Next, the phenomena occurring during electroetching using these current waveforms as the second stage will be explained in detail using Figure 2.

[0059]

At the stage when first-stage electrolysis has ended, a metal conductor is formed not only in holes or channels having residual metal conductor, but also on the dielectric surrounding these. Therefore, the metal conductor in these parts must be selectively removed. The method used for this is the electroetching described below:

[0060]

To dissolve and remove unnecessary metal as far as the dielectric surface while keeping the uniform and flat plated surface over the entire surface described above flat and smooth, this may be subjected to electroetching by current reversal electrolysis by reversing the relative times of i_cT_c and i_aT_a determined by the current waveforms shown in Figures 2(a), 2(b), and 2(c) and making effective current i_e positive; that is, an anode current. That is, dissolution and electrodeposition are alternated by pulses as before, but this time, dissolution is increased over electrodeposition so that dissolution (etching) occurs

preferentially overall. By this method, the flat plating surface formed by the electrodeposition process of the first stage is etched uniform and flat, and a flat thin-film circuit pattern can be formed with a conductor packed in only fine holes or channels in the substrate surface.

[0061]

Preferred current waveform conditions at this time are a frequency of 1 Hz to 1 MHz and an effective electrodeposition current of 0.1 to 10 A/dm^2. This is because less than 1 Hz frequency differs little from direct-current electrolysis and cannot achieve the advantages of this method, while greater than 1 MHz frequency cannot track reaction of metallic ions in the plating solution and does not cause plating. Furthermore, less than 0.1 A/dm^2 effective electrodeposition current increases step time too much and is impractical, while greater than 10 A/dm^2 current has problems such as tending to simultaneously generate hydrogen and tending to produce defects.

[0062]

Moreover, the two steps described above — namely, a plating step and an electroetching step — may be performed continuously in the same plating solution, or in separate processing solutions differing in composition.

[0063]

[Concrete Process Conditions and Details of Production Steps]

[Working Examples 1 to 3]

Concrete process conditions and details of production steps in working examples with which this invention is concerned will be explained below using Figure 5. Figure 5 is a diagram showing steps in the production method of one working example with which this invention is concerned.

[0064]

These Working Examples 1 to 3 are designed such that a conductor material is ultimately buried in only the holes or channels of a pattern of fine holes or fine channels on a dielectric surface, and a flat thin-film circuit pattern is formed. Details of the process conditions of each working example are shown together in the following Table 1.

[0065]

[Table 1]

Step Diagram	Process	Working Example 1	Working Example 2	Working Example 3
Figure 5(a)	substrate	mullite glass ceramic substrate, thickness: 1 m	same	same
Figure 5(b)	dielectric film formation	1) Polyimide PID manufactured by Hitachi Chemical Co., Ltd.: spin-coat, heat-cure (full cure) 2) thickness: 20 :m	same	1) Polyimide PL-2035 manufactured by Hitachi Chemical Co., Ltd.: spin-coat, heat-cure (full cure)
Figure 5(c)	dielectric film pattern working	dry etching using Al film as mask 1) working conditions: parallel plate RIE apparatus, 0_2 RIE, O_2 gas pressure = 1 mmTorr 2) working dimensions: minimum via diameter = 5 :m, minimum channel width = 5 :m 3) Al mask removal: aluminum sulfide etchant	dry etching using Al film as mask 1) working conditions: KrF excimer laser 2) working dimensions: minimum via diameter = 5 :m, minimum channel width = 5 :m 3) Al mask removal: aluminum sulfide etchant	1) exposure: 1:1 projection aligner 2) developing: puddle method 3) heat curing: full cure (final thickness: 10 :m) 4) working dimensions: minimum via diameter = 10 :m, minimum channel width = 10 :m
Figure 5(d)	electroplating underlayer formation	sputtering film formation:-sputter-etch just before film formation. Cr (500 Å) / Cu (5000 Å)	same	same
Figure 5(e)	electroplating (current reversal electrolysis)	1) plating solution: acidic sulfuric acid copper plating $CuSO_4 \cdot 5H_2O$: 60 g/L H_2SO : 200 g/L brightener: small amount 2) electrolysis conditions: frequency = 1.5 kHz $i_e = -2.0$ A/dm Cu thickness on dielectric = 10 :m	1) plating solution: acidic sulfuric acid copper plating $CuSO_4 \cdot 5H_2O$: 60 g/L H_2SO : 200 g/L brightener: small amount 2) electrolysis conditions: frequency = 1.0 kHz $i_e = -3.0$ A/dm Cu thickness on dielectric = 10 :m	same
Figure 5(f)	electroetching (current reversal electrolysis)	1) treatment solution: above-mentioned plating solution used as appropriate 2) electrolysis conditions: frequency = 1.5 kHz $i_e = +0.5$ A/dm^2	1) treatment solution: above-mentioned plating solution used as appropriate 2) electrolysis conditions: frequency = 1.5 kHz $i_e = +0.5$ A/dm^2	same
Figure 5(g)	pattern separation	1) Cr etching: alkaline potassium ferricyanide solution	same	

[0066]

The course of production steps will be explained below: First, dielectric film 22 comprised of organic resin is grown on top of ceramic substrate, glass substrate, or organic resin substrate 21 (Figures 5(a) and (b)). A polyimide film, epoxy resin film, or other heat-resistant resin film can be used for the organic resin. For the film formation method, the method of coating a varnish of said resin by a means such as spin-coating, printing, or spraying, then drying and heat-curing may be used, or the method of heat-pressing a film of said resin may be used. Moreover, a photosensitive polyimide or photosensitive epoxy resin that is itself photosensitive may be used for the material of this dielectric film.

[0067]

Next, a pattern of fine holes or channels is worked onto dielectric film 22 (Figure 5(c)). If the material is a non-photosensitive resin film, a method such as dry etching using a metal mask or laser ablation by an ultraviolet laser can be used for the working method. If a photosensitive resin such as a photosensitive polyimide or photosensitive epoxy resin is used, a resin-film pattern can be formed directly by a photolithography step. Figure 5(c) shows the status after working the organic resin film, and shows locations where holes or channels have a vertical cross-section. When the working method is dry etching or laser ablation, the side walls are roughly perpendicular as shown in Figure 5(c), while when a photosensitive resin is used for the dielectric film, the side walls are tapered.

[0068]

In the next, step, an underlayer is formed for use as a charge layer during electroplating (Figure (d)). Examples of formation methods for this underlayer include the method of forming a laminated film of Cr/Cu or Ti/Cu by continuous deposition, and the method of forming a Cu film by electroless plating. Cr and Ti here play the role of a tight adhesion layer with the underlayer dielectric film, while Cu plays the role of a charge layer.

[0069]

EB deposition or sputtering can be used for the above continuos deposition, but sputtering is superior from the standpoint of producing tight adhesion. In particular, to securely reduce all contact resistance of innumerable via within the plane and eliminate any contact failure, the floor of via holes must be cleaned by a sputter-etch step before film formation. Therefore, the sputtering apparatus must be an apparatus having a sputter-etch mechanism. The surface may be sputter-etched inside the vacuum chamber of the apparatus before film formation, then subjected to film formation continuously without moving.

[0070]

Moreover, the thickness of the tight adhesion film of Cr and Ti is preferably about 300 to 1500 Å, and the thickness of Cu used as a charge layer is preferably about 1000 to 10,000 Å.

[0071]

In the next step, the surface is subjected to flattening plating and flattening electroetching by the current reversal electrolysis method described above (Figures 5(e) and (f)). An acidic sulfuric acid copper plating solution can be used for the electrolysis solution, and a material such as Teflon or hard vinyl chloride

can be used for the electrolysis reaction tank.

[0072]

The configuration of the electrolysis system can realized as described in the previous section [Configuration of Electrolysis System for Reducing This Invention to Practice].

[0073]

As described already, the current waveform conditions of frequency in a range of 1 Hz to 1 MHz and effective current in a range of 0.1 to 10 A/dm^2 (absolute value) are preferred in both electroplating mode and electroetching mode, and optimum conditions may be selected from within these ranges. In the present working examples, ending anode dissolution of copper electroplating film produces the status shown in Figure 5(f), and electroplating underlayer film 23 is exposed. If Cr/Cu or Ti/Cu is used as electroplating underlayer film 23, Cu is etched together with the electroplating copper at this time, leaving Cr or Ti exposed on electroplating underlayer film 23 shown in Figure 5(f). Because the acidic sulfuric acid copper plating solution is strongly acidic, elements such as Cr or Ti are slightly etched, but as etching progresses, the pattern becomes discontinuous and inevitably produces an etching residue. Therefore, to securely separate the hole or channel pattern from the plane around it, this is preferably subjected to selective chemical etching that selectively dissolves Cr and Ti and does not dissolve Cu at the final stage.

[0074]

Moreover, electroplating and electroetching are preferably applied continuously in the same electrolytic tank from the standpoint of streamlining steps, but these may be applied in separate electrolytic tanks using different electrolyte solutions.

[0075]

In addition, the electroetching step may be replaced by a step such as electrolytic polishing. As electrolytic polishing conditions, electrolytic polishing may be applied using 63% phosphoric acid and a current density in a range of 10 to 60 mA/cm^2.

[0076]

The configuration shown in Figure 5(b) can be formed by the series of steps described above. That is, a copper plating conductor can be packed into only the holes or channels of a dielectric surface having a pattern of fine holes or fine channels, and a thin-film circuit pattern having a flat surface can be formed. As a gauge of the flatness of said thin-film pattern surface, if the via height is 20 :m, the step difference of the via part (the difference between dielectric film 22 and electroplating conductor 25 in Figure 5(g)) can achieve a mean of about 0.4 :m and a maximum of about 1.1 :m. These values are low enough to form a thin-film multilayer circuit board by this process.

[0077]

[Working Example 4]

Another working example with which this invention is concerned will be explained below using Figure 6. Figure 6 shows substrate sections showing steps of the production method of another working example with which this invention is concerned.

[0078]

This Working Example 4 pertains to production of a thin-film multilayer circuit board using the thin-film circuit formation process described above.

[0079]

The course of production steps will be explained below:

[0080]

Multilayer ceramic substrate 331 is formed by simultaneously sintering a layout conductor metal and a ceramic material. A substrate such as a mullite-tungsten simultaneously-sintered substrate or glass ceramic-copper simultaneously-sintered substrate can be used for the multilayer ceramic substrate. Because the surface of the multilayer ceramic substrate has warping and irregularities caused by ceramic grains, it cannot be used as is in the following thin-film steps. Therefore, the substrate surface is worked by lapping and polishing to a level of 5 :m or less warping and 0.1 :m or less surface roughness Ra. First, adjusting pad 313 is formed on this surface (Figure 6(a)). An "adjusting pad" is a thin-film electrode installed to assure continuity with the thin-film layout by absorbing any pattern deviation due to irregular shrinkage of the ceramic substrate during sintering. A multilayer film comprised of Cr (1000 Å) / Cu (5 :m) / Cr (500 Å) formed by sputtering is used to form adjusting pad 313. This can be worked to the desired shape by photoetching.

[0081]

Next, organic resin insulating film 314, which becomes the first layer, is formed on the upper surface of this multilayer ceramic substrate 331 and adjusting pad 313 (Figure 6(b)). A resin such as polyimide, epoxy resin, photosensitive polyimide, or photosensitive epoxy resin can be used as the material. If polyimide or epoxy resin is used, this can be subjected to dry etching using a metal mask or laser ablation by an ultraviolet laser in the next step (Figure 6(c)) as described in Working Examples 1 to 3.

[0082]

If a photosensitive organic resin insulating film such as photosensitive polyimide or photosensitive epoxy resin is used, the film itself can be exposed directly and worked into a pattern by photolithography. This is useful in terms of shortening steps compared to the complex steps of forming a photoresist, patterning and etching the photoresist, and peeling the photoresist used to form a pattern when a non-photosensitive organic resin insulating film is used.

[0083]

An example using photosensitive polyimide PL-2035 manufactured by Hitachi Chemical Co., Ltd.

will be explained here. After spin-coating and pre-baking a varnish of PL-2035, a coat with a thickness of 20 :m can be obtained. Via formation is completed by exposing and developing this in a pattern under set conditions, then finally heat-curing in a hot air furnace. Resin thickness after heat-curing is 10 :m, and a minimum via size of 10 :m can be achieved.

[0084]

Next, organic resin insulating film 316, which becomes the second layer, is formed in the same way as the first layer (Figure 6(d)). Layout channels are worked in photosensitive polyimide at this stage, but because the film is thicker in the first-layer via parts, these parts tend to be difficult to develop. Therefore, developing conditions are reinforced by employing repeated puddle developing or ultrasonic developing, and conditions are established that do not produce developing residue. At this point, a depression pattern combining via and the layout is formed on the surface of organic resin insulating film.

[0085]

Next, a laminated film of Cr (500 Å) / Cu (5000 Å) is sputtered and formed as an electroplating underlayer (Figure 6(e)).

[0086]

Next, this underlayer film is subjected to flattening plating by current reversal electrolysis (Figure 6(f)). A sulfuric acid copper plating solution is used for the plating solution, and the same system as in Working Examples 1 to 3 is used for the electrolysis system. Electrolysis is applied selecting a frequency in a range of 1 Hz to 1 MHz and an effective current in a range of –1 to –10 A/dm^2 as electrolysis conditions, and a copper plating film is formed having a flat surface as shown in Figure 6(f).

[0087]

Next, this is subjected to flattening electroetching by current reversal electrolysis in the same electrolyte solution. For this, a frequency is selected in a range of 1 Hz to 1 MHz, and an effective current is selected in a range of –1 to –10 A/dm^2.

[0088]

Furthermore, the underlayer film of a tight adhesion layer of Cr remaining on the surface in the electroetching step can be removed by a selective etching solution such as alkaline potassium ferricyanide solution to obtain the status shown in Figure 6(g). That is, a copper conductor can be packed without gaps into the pattern of via and layout channels formed in organic resin insulating film, and a thin-film circuit having a flat surface can be formed.

[0089]

An extremely high-density thin-film multilayer circuit board can be formed by forming an organic resin insulating pattern such as Figure 6(h) on top of this, then repeating steps from Figure 6(c) to Figure 6(g) the number of times required (exactly the number of layout layers).

[0090]

Moreover, if the material of this organic resin insulating film is formed by coating a polyimide varnish or photosensitive polyimide varnish when forming a pattern on this organic resin insulating film 320, a reaction product between copper and the polyamic acid that is the resin component of these varnishes may be formed on the layout surface of electroplating copper 319. This reaction product remaining on via floor 321 in the pattern formed on organic resin insulating film 320 (Figure 6(h)) causes increased via contact resistance.

[0091]

To solve this problem, in this working example, satisfactory via contacts can be obtained by implementing the following reaction preventing measure at the stage of Figure 6(h):

[0092]

1) Oxygen plasma treatment or 2) chromate treatment is applied as a copper-polyimide reaction prevention measure.

[0093]

Oxygen plasma treatment is applied using a barrel-shaped asher under treatment conditions of 0.5 Torr oxygen gas pressure, 300 W RF output, and two minutes treatment time. Oxygen plasma treatment leaves a copper oxide coating on the floor of organic insulating film via. Therefore, after working via, via are subjected to a dilute sulfuric acid treatment (immersing in 5% sulfuric acid for one to two minutes, then washing with water) to remove the copper oxide coating.

[0094]

Chromate treatment is applied by immersing in 1 to 2% aqueous solution of heavy potassium chromate for one to two minutes at room temperature, then washing with water. Preferably, the chromate coating on via floor 321 after chromate treatment is removed, which is done by treating with an aqueous solution of alkaline potassium ferricyanide.

[0095]

Introducing the reaction preventing measures described above can achieve a via contact resistance of 2 mΩ/via or less.

[0096]

[Working Example 5]

Another working example with which this invention is concerned will be explained below using Figure 7. Figure 7 is a section of a thin-film multilayer circuit board with which one working example of this invention is concerned and an LSI mounting structure using this circuit board.

[0097]

This Working Example 5 offers a mounting structure and electronic device for mounting an

integrated circuit element (LSI) on the high-density thin-film multilayer circuit board realized in Working Example 4. First, an electrode for soldering is formed on the uppermost layer of the thin-film multilayer circuit board formed in Working Example 4. This electrode for soldering is comprised of lower connecting electrode 418 and upper connecting electrode 419. This lower connecting electrode 418 uses a Cr/Cu/Cr laminated film formed by sputtering, and is worked into a cylindrical electrode by photoetching.

[0098]

Next, surface-layer organic resin insulating film 423 is formed. Either a non-photosensitive or a photosensitive resin may be used for the material of surface-layer organic resin insulating film 423. Connection holes are worked in this, but any of the methods described in Working Examples 1 to 3 can be used for the working method depending on the material.

[0099]

The side walls of the holes in organic resin insulating film 415 play the role of a solder dam during soldering in the next step. In addition, because these side walls are placed inside the edges of lower connecting electrode 418, this placement prevents stress due to soldering from concentrating on the edges of lower connecting electrode 418, and is useful in terms of improving reliability.

[0100]

Next, the Cr film on the surface of lower connecting electrode 418 is removed by the selective etching solution described earlier, and the surface of the Cu film is exposed. This is subjected to palladium activation treatment, then to electroless Ni-B plating or electroless Ni-P plating. In addition, this surface is subjected to substitution gold plating, and if required, a further 0.5 to 2.5 :m gold plating film is formed by electroless gold plating.

[0101]

The steps described above complete a high-density thin-film multilayer circuit board for mounting an LSI, including a surface contact electrode. In particular, because via 414 in the thin-film multilayer circuit board has a flat surface and via 414 can easily be formed vertically, a layout pattern can be mounted at extremely high-density.

[0102]

Fine solder ball 420 is supplied to the connecting electrode of the thin-film multilayer circuit board described above, LSI 422 having similar LSI connecting electrode 421 in a position opposite this connecting electrode is mounted on top of this while mutually positioning these, and the two electrodes are connected by passing through a heating furnace to melt the solder. This can realize an electronic circuit device having extremely many pins and ultrahigh integrated LSI mounted with great reliability.

[0103]

Moreover, this mounting structure can be used for single chip packages as well as multi-chip packages.

[0104]

[Effects of the Invention]

According to this invention, a metallic conductor is ultimately packed in only the holes and channels without gaps and at a higher density than in prior art when applying metallization to a dielectric surface having holes and channels formed in a pattern in the production process of a high-density, thin-film, multilayer circuit board, and this conductive surface is made uniform and coplanar with the surface containing the above-mentioned dielectric surface. In addition, this invention achieves complete flatness in each layer comprising a thin-film multilayer circuit board, facilitates multilayering a thin-film circuit, and greatly improves mounting density while maintaining high yield.

[Brief Explanation of the Figures]

Figure 1 is a schematic diagram showing the configuration of an electrolysis system for implementing the electrolysis with which this invention is concerned.

Figure 2 is a graph showing the correlation between current density and time in current reversal electrolysis with which this invention is concerned.

Figure 3 is a schematic diagram contrasting an electrolytic bath with its metal concentration.

Figure 4 is a diagram contrasting how the surface on a substrate varies when plated by direct current or a pulse current.

Figure 5 is a diagram showing steps in the production method of one working example with which this invention is concerned.

Figure 6 is a diagram showing steps of the production method of another working example with which this invention is concerned.

Figure 7 is a section of a thin-film multilayer circuit board with which one working example of this invention is concerned and an LSI mounting structure using this circuit board.

Figure 8 is a diagram showing contrasting sections of thin-film multilayer circuits having via.

[Explanation of Reference Numbers]

a ... organic resin insulating film

b ... layout conductor

c ... electroplating underlayer

d ... electroplating layout conductor

e ... electroless plating via

i_c ... cathode current

i_a ... anode current

i_e ... effective current

T_c ... cathode current pulse width

T_a ... anode current pulse width

T_1 ... rest time

T_2 ... rest time

21 ... substrate

22 ... dielectric film

23 ... electroplating underlayer

24 ... hole or channel

25 ... electroplating conductor

311 ... ceramic

312 ... thick-film through-hole conductor

313 ... adjusting pad

314 ... organic resin insulating film (1)

315 ... via hole

316 ... organic resin insulating film (2) [after forming channel pattern]

317 ... channel pattern

318 ... electroplating underlayer

319 ... electroplating copper

320 ... organic resin insulating film (3) [after forming via hole pattern]

321 ... via floor

411 ... thick-film through-hole conductor

412 ... ceramic

413 ... adjusting pad

414 ... via

415 ... organic resin insulating film

416 ... X-direction layout

417 ... Y-direction layout

418 ... lower connecting electrode

419 ... upper connecting electrode

420 ... solder

421 ... LSI connecting electrode

422 ... LSI

423 ... surface-layer organic resin insulating film

[Figure 1]

Figure 1

511 ... control personal computer
512 ... desired signal waveform generator
513 ... constant-current constant-voltage pulse source
514 ... electrolytic bath
515 ... electrolyte solution
516 ... substrate holder and substrate
517 ... counter-electrode

[Figure 2]

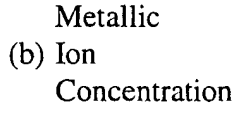
Figure 2

i_c ... cathode current
i_a ... anode current
i_e ... effective current
T_1 ... rest time
T_c ... cathode current pulse width,
T_a ... anode current pulse width
T_2 ... reset time

[Figure 3]

Figure 3

(a)



Distance from Deposited Surface

514 ... plating solution, 516 ... substrate, 517 ... counter-electrode, A ... deposited surface, B ... before plating, C ... diffusion layer, D ... plating solution bulk layer

[Figure 7]

Figure 7

411 ... thick-film through-hole conductor 412 ... ceramic 413 ... adjusting pad
414 ... via 415 ... organic resin insulating film 416 ... X-direction layout
417 ... Y-direction layout 418 ... lower connecting electrode 419 ... upper connecting electrode 420 ... solder 421 ... LSI connecting electrode 422 ... LSI
423 ... surface-layer organic resin insulating film

[Figure 4]

Figure 4

A ... during plating → after plating, B ... diffusion layer, C ... plating film, D ... direct current, E ... substrate, F ... pulse current

[Figure 5]

Figure 5

21 ... substrate
22 ... dielectric film
23 ... electroplating underlayer
24 ... hole or channel
25 ... electroplating conductor

[Figure 6]

Figure 6

311 ... ceramic
312 ... thick-film through-hole conductor
313 ... adjusting pad
314 ... organic resin insulating film (1)
315 ... via hole
316 ... organic resin insulating film (2) (after forming channel pattern)
317 ... channel pattern
318 ... electroplating underlayer
319 ... electroplating copper
320 ... organic resin insulating film (3) (after forming via hole pattern)
321 ... via floor

[Figure 8]

Figure 8

a ... organic resin insulating film
b ... layout conductor
c ... electroplating underlayer
d ... electroplating layout conductor
e ... electroless plating via

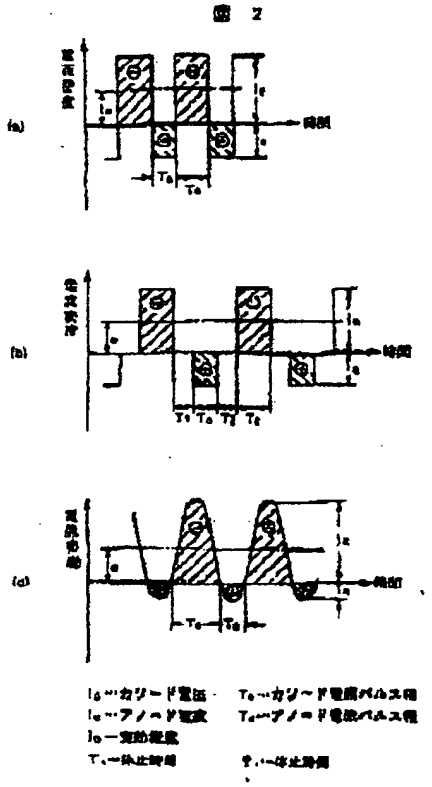
ATTN: HUGH JOB 01555

JP 9533017A Machine Translation

【図２】

[Figure 2]

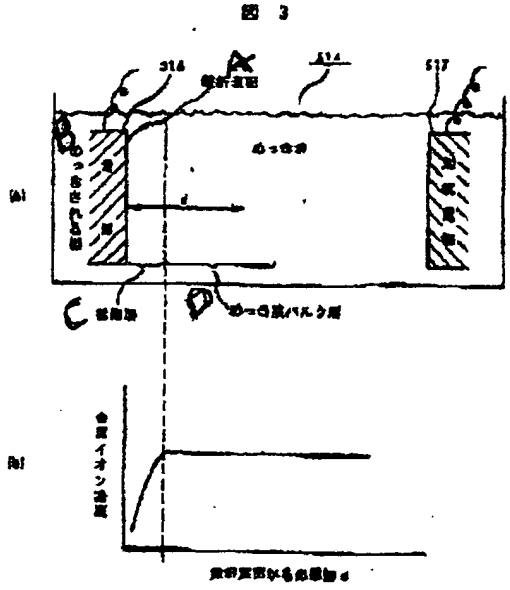
図 2



【図３】

[Figure 3]

図 3

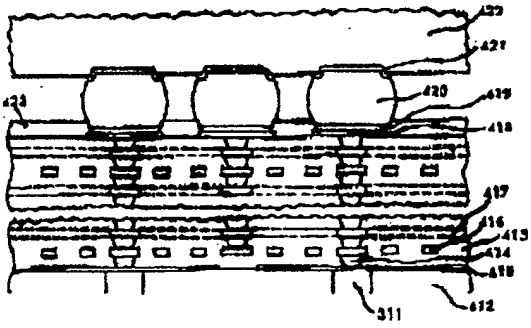


JP 9533601 7A Machine Translation

【図７】

[Figure 7]

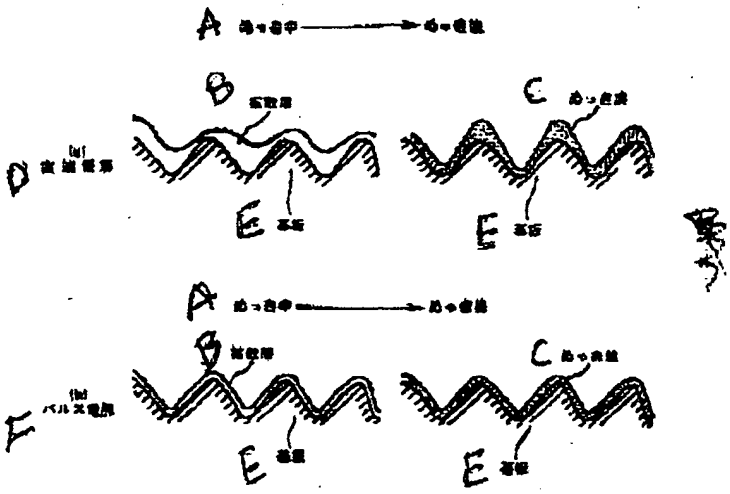
図 7



411—[illegible] 412—セラミック 413—[illegible]
414—ビア 415—[illegible] 416—X方向配線
417—Y方向配線 418—[illegible] 419—[illegible]
配線 420—半田 421—LSI[illegible] 422—LSI
423—[illegible]

【図４】

[Figure 4]



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DN S51343-EP	01310721.4-2119-

Anmelder/Applicant/Demandeur/Patentinhaber/Proprietor/Titulaire
Shipley Co. L.L.C.

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If applicable, copies of the documents cited in the European search report are attached.

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The following specifications given by the applicant have been approved by the Search Division:

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☐ The abstract was modified by the Search Division and the definitive text is attached to this communication.

The following figure will be published together with the abstract: NONE

REFUND OF THE SEARCH FEE

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EUROPEAN SEARCH REPORT

Application Number
EP 01 31 0721

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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X	US 5 151 170 A (MONTGOMERY EDA R ET AL) 29 September 1992 (1992-09-29) * column 1-2 * * examples 1-3 *	1-7,9-12	
X	US 4 347 108 A (WILLIS WILLIAM J) 31 August 1982 (1982-08-31) * claims 1-6,14,17 * * column 2, line 36 - column 3, line 48 *	1-6,9-12	
X	US 4 134 803 A (ECKLES WILLIAM E ET AL) 16 January 1979 (1979-01-16) * column 2, line 61 - column 3, line 60 *	1-6,9-12	
X	US 3 798 138 A (OSTROW B ET AL) 19 March 1974 (1974-03-19) * column 1, line 15 - column 3, line 6 * * claims 1-4,13,14 *	1-6,9-12	
A	DE 32 40 643 A (LPW CHEMIE GMBH) 30 May 1984 (1984-05-30) * abstract; examples 1,2 *	1,8	

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C25D

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	2 May 2002	Haering, C

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 31 0721

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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